180nm HV18, HV30, UHV$_{PLUS}$ Process Technologies

GLOBALFOUNDRIES 180nm High Voltage process technologies, including HV18, HV30 and UHV$_{PLUS}$, are part of a modular platform architecture based on the company's logic process baseline, integrating power and high voltage transistors, precision analog passives. This process offers superior cost and performance for HVCMOS and AC/DC applications, such as:

- Off-line (AC-connected) LED lighting
- LED backlighting for monitors/TVs
- AC-DC (chargers, adapters, white goods, etc.)
- HVCMOS controller for MEMS
- Wireless charging

LED light bulbs

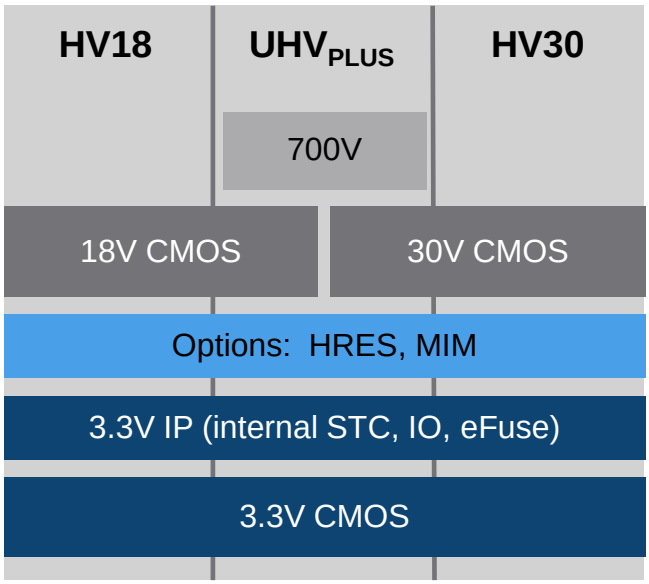
AC Adapter

Wireless charging

Process Features

- 3.3V LV CMOS with 180nm BEOL
  - High CMOS density reduces digital blocks by 50% (compared to 350nm technology)
  - 3.3V for optimal analog circuit performance
  - Well suited for Digital Power Management
  - In-house IP for digital standard cells, eFuse, GPIO, ESD
- HVCMOS with 180nm design rules for reduced footprint
  - 18V and 30V CMOS options to meet end-customer specs
- Additional features
  - Rated at 150ºC to accommodate high ambient temperature applications
  - 1.2µm and 3.0µm thick top metal options allow Cu-wire bonding (non-CUP and CUP)
- Extensions
  - UHV$_{PLUS}$ adds 700V normally-ON and normally-OFF LDMOS
  - Allows easy integration of start-up and self-powering functions to existing controllers

Modular Process, Integrated PDK

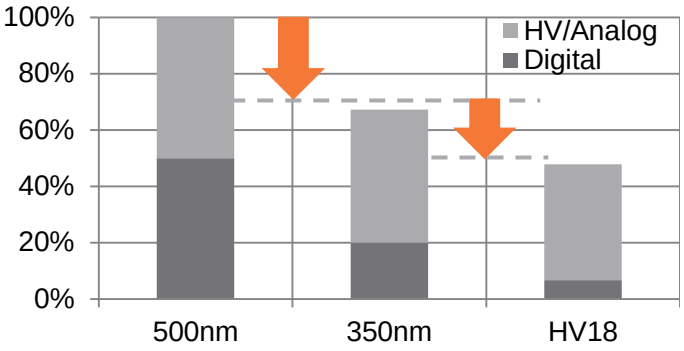


30% Die Size Shrinks

Consecutive 30% die size shrinks when migrating from 500nm to 350nm to HV18 due to tighter back-end design rules and shallow trench isolation

	500nm	350nm	HV18
Digital circuit density (k-gates / mm²)	8	20	70
18V CMOS device pitch	5.50	5.20	4.52

Consecutive 30% Die Size Shrinks from 500nm to 350nm to HV18



Assuming 50% digital and 50% HV/analog

EDA/IP Solutions

	180nm HV18	180nm HV30	180nm UHV_{PLUS}
3.3V Standard Cells	GLOBALFOUNDRIES		
3.3V I/O	GLOBALFOUNDRIES		
eFuse	GLOBALFOUNDRIES		
Circuit Simulation	Synopsys / Cadence		
Spice Model	BSIM4.5 with Sub Ckt		
PDK	Cadence		
DRC/LVS	Mentor		
RCX	Mentor / Synopsys / Cadence		
ESD Library	GLOBALFOUNDRIES		
Digital Design Flow	Synopsys / Cadence		

180nm HV18 Process Architecture

- 3.3V CMOS low mask count baseline process, includes all GLOBALFOUNDRIES IPs
- 18V or 30V CMOS with thicker gate oxide (Vgs = ± 18/30V, Vds = ± 18/30V)
- 700V NMOS uses 18V or 30V oxide (Vgs = ± 18/30V, Vds = + 700V)
- UHV devices: enhancement MOS (normally-OFF), depletion MOS (normally-ON)