

Designing into a Foundry Low Power High-k Metal Gate 28nm CMOS Solution for High-Performance Analog Mixed Signal and Mobile Applications

A Collaborative White Paper by RAMBUS
and GLOBALFOUNDRIES

W H I T E P A P E R



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Introduction – High-k Metal Gate CMOS Low Power Solutions

28nm Super Low Power (28nm-SLP) is the low power CMOS offering delivered on a bulk silicon substrate for mobile consumer and digital consumer applications. GLOBALFOUNDRIES' 28nm-SLP process technology is designed for the next generation of smart mobile devices, enabling designs with faster GHz processing speeds, higher circuit density, lower standby power and longer battery life. The 28nm process technology is slated to become the foundation for a new generation of portable electronics that are capable of handling streaming video, data, voice, social networking and mobile commerce applications.

This technology has four V_t 's (high, regular, low, and super low) for design flexibility with multi-channel length capability and offers the ultimate in small die size and low cost. Multiple SRAM bit cells for high density (smallest in the industry) and high-performance are available. With the simpler process integration of a "Gate-First" HKMG scheme, 28nm-SLP also offers the use of an eFuse which is known to be more competitive and superior than a BEOL (Back End Of Line) copper fuse solution.

28nm-SLP is a lower cost technology relative to other 28nm options, being manufactured without the stress elements used to boost carrier mobility for 28nm poly SiON and for 28nm HKMG HP (high-performance) technologies, reducing process complexity and mask count substantially.

Implementing Rambus Innovations in 28nm-SLP Technology

Rambus demonstrated the readiness of 28nm-SLP process by successfully completing multiple tape-outs implementing Rambus innovations. The versatile platform was used to design both high performance PC main memory and low power mobile memory

systems. These tape-outs demonstrated the results of a close collaboration between Foundry technologists and Rambus designers in delivering a Low Power and High Speed Memory Interface for key market areas such as low power, mobile, graphics, computer and consumer electronics segments.

Design implementation was done utilizing the qualified reference flows, partner IP and verified for manufacturability using both pattern matching and model based DFM solutions. Finally, the chips utilized GLOBALFOUNDRIES' turnkey services in delivering both wirebond and flip chip solutions. Packaging flexibility is a key enabler for high performance and low power IO systems and GLOBALFOUNDRIES' expertise proved invaluable in implementing multiple packaging options.

28nm-SLP Technology Attributes for Superior Analog Performance

The GLOBALFOUNDRIES' 28nm-SLP process offers analog mixed-signal designers a great degree of design freedom to meet all aggressive circuit block specifications. The 28nm-SLP process technology allows Rambus memory system designers to meet the constraints of a fixed power envelope while pushing performance.

Availability of Multi-Channel Multi-Vt Transistors

Unlike some other advanced processes, a continuous range of channel lengths can be used to optimize different circuit classes independently. Availability of four different threshold (Vt) options allows design optimizations at various levels of design hierarchies. At higher levels, it allows minimization of leakage power for non-critical circuits and achievement of highest speed and lowest sensitivity to supply noise for critical paths, clocking, and bit rate circuits. At lower levels, it enables designs of low-leakage,

high-performance, power gated circuits, and it allows optimization of current sources, mirrors, and other analog circuits where gate overdrive, saturation margin, output impedance, and matching are of utmost importance. The availability of the super low V_t transistor tilts the scale from an HP process to the SLP process for a performance-minded product where power is also a first-order concern.

Passive Devices and Noise Models

In terms of passive device availability, GLOBALFOUNDRIES provides a rich offering of parameterized layout and matching HSPICE models. Some of the more unique devices that Rambus was able to leverage included a symmetric, spiral inductor, both P and N varactors, and a higher precision (sheet rho variability) resistor with a higher nominal sheet resistance. The availability of these cells and models decreased the design time required by RAMBUS, allowed lower power design points, and increased Rambus' confidence in first silicon success. In addition, GLOBALFOUNDRIES' PDK provided early support for silicon calibrated $1/f$ noise and high frequency (thermal) noise models.

Device Variability

With each new process generation, global and local device variations become even more of a primary concern for the mixed-signal designer. The GLOBALFOUNDRIES' PDK includes a comprehensive set of HSPICE models that can be used in numerous ways to model wafer-to-wafer variation, within die variation including matching, and both simultaneously. These models allow designers to achieve robust design without being overly pessimistic – minimizing costs of overdesigns such as unnecessary power consumption and/or silicon area.



ESD

For high-speed IO design, minimization of ESD capacitance to meet standard zap models is paramount. GLOBALFOUNDRIES' SPICE models include special ESD device models that capture effects necessary for proper simulation of ESD events that are not typically part of a generic diode model, for example. Robust ESD structures using the modeled devices are also part of the PDK. Both DRC and PERC rules are also provided by the foundry to protect the designer from making poor choices in ESD and multiple power domain design.

Overdrive Transistors

The process also allows a 1.15V overdrive of the nominal 1V smallest oxide thickness transistors. This was taken full advantage of for on-chip supply regulators where trade-offs of regulated supply voltage level and power supply noise rejection had to be balanced. While multiple options for IO voltages are generally nice to have, overdrive and underdrive capability of the transistors can simplify technologies' transistor offerings.

Utilizing the Design Enablement Solutions for 28nm-SLP

GLOBALFOUNDRIES offers a rich and comprehensive Process Design Kit (PDK) for its customers' use, and collaborates with its Common Platform partners and multiple ecosystem partners in EDA and IP to deploy a design enablement ecosystem for 28nm with EDA tool flows, ARM standard cell libraries, memory compilers, I/O, and advanced IP blocks. The PDK contains GLOBALFOUNDRIES-provided 28nm process models and process data in the appropriate Cadence technology file formats to enable fast and silicon-accurate IC design in the Cadence Virtuoso custom design platform. The PDK is also supported by GLOBALFOUNDRIES' AMS reference flow, which includes

both Custom and Encounter Digital Platform based flow, with detailed flow documentation and proven results from prior test chip silicon. PDK support documentation is quite detailed and efficient with multi-level hierarchy with full support for simple to more complicated usage and expertise. Rambus benefitted greatly from using the PDK by streamlining the design process and reducing the amount of rework during time-sensitive tape-out processes. Overall, the PDK and AMS reference flow provided fast, silicon-accurate design enablement solutions for both front-end to back-end flow and helped the Rambus team design for power, performance and area.

Utilizing DRC+

Design for Manufacturability (DFM) requirements have been a barrier for many design teams who are thinking about moving to lower process nodes. But can DFM actually get easier as process nodes shrink? That possibility is offered by DRC Plus (DRC+), a new technology developed by GLOBALFOUNDRIES in collaboration with Cadence and Mentor Graphics.

DRC+ is a pattern-based DFM methodology that can be run “in design” by chip design teams well before tape-out. It works much like standard Design Rule Checking (DRC), but instead of just coding rules, it uses shape-based pattern matching to identify layout configurations that could be difficult to manufacture. DRC+ rules are comprised of a yield detracting pattern library to avoid and a recommended DFM rule to follow. Designers fix violations by avoiding the pattern or enforcing the rule. DRC+ allowed Rambus fast detection of problematic litho patterns while providing automatic fix capability. Rambus was able to incrementally verify and fix DFM violations as part of its design process prior to final tape-out.

Utilizing GLOBALFOUNDRIES' Assembly Solutions

Rambus utilizes multiple packaging solutions to demonstrate both low cost and high-performance assembly options for its high speed PHYs. Having a foundry specialize and provide multiple advanced assembly solutions is therefore very beneficial. GLOBALFOUNDRIES has deep expertise in advanced assembly solutions and offers design consulting to its customers. Rambus engages with GLOBALFOUNDRIES to provide wirebond and flip chip packaging options on high speed PHY designs. Rambus' technology team worked with the foundry team in Singapore to create a custom packaging flow for Rambus designs taking into account unique requirements, such as the use of a single GDS tape-out and strict RDL width-space constraints. Multiple IO pad options are available in the IO library offered by ecosystem partners, thereby allowing tight pitch selection in keeping with 28nm scaling. Depending upon the design requirements, both lead-free and eutectic material options are available and Rambus utilized both options for multiple chip tape-outs. Big complex designs are also complicated by the need for process splits and different assembly options, both of which are logistically supported very well by the foundry. The selection of OSAT based on the requirements was transparent to the design team and the resulting cycle time communicated early on to the design team.



Conclusions

Rambus designs silicon robust IP and therefore requires high-performance silicon technology to demonstrate industry leading data rates. In addition to performance, analog-MS designs place additional requirements for precision and parametric control. The 28nm Super Low Power (SLP) technology presents tremendous value for the industry in that it meets demanding performance-scaling needs from 40nm, and provides an outstanding platform for analog mixed signal design. The design enablement solutions offered by GLOBALFOUNDRIES are supported by leading EDA vendors, well proven to reduce risk, enable thorough full-chip verification while promising first time working silicon.

Reduced risk is a hallmark of this low power technology. Lowered risk is realized on several fronts – (1) proven high-volume manufacturing is available at multiple Common Platform Alliance locations globally, (2) a fully enabled design ecosystem with IP and tools and proven design flows, available today, (3) sustaining of the industry design style, flexibility and infrastructure utilized at 40nm and all previous technology nodes, (4) superior performance and analog headroom for wider design margin, and (5) lower manufacturing cost.

True collaboration between a fabless design/IP company and the foundry is required to promote early adoption of a new technology node. Rambus and GLOBALFOUNDRIES maintained an open communication channel throughout the design cycle with frequent communication between the Rambus foundry team and GLOBALFOUNDRIES technology experts. Access to leading-edge technology, ecosystem partners, foundry experts and proven design enablement is a precursor of a successful technology adoption. Rambus and GLOBALFOUNDRIES demonstrated such a partnership in proving the versatility and robustness of 28nm-SLP platform to the industry.



ABOUT RAMBUS

Founded in 1990, Rambus is one of the world's premier technology licensing companies. As a company of inventors, Rambus focuses on the development of technologies that enrich the end-user experience of electronic systems. Its breakthrough innovations and solutions help industry leading companies bring superior products to market. Rambus licenses both its world-class patent portfolio, as well as its family of leadership and industry standard solutions. Headquartered in Sunnyvale, California, Rambus has regional offices in North Carolina, Ohio, India, Germany, Japan, Korea, and Taiwan. Additional information is available at www.rambus.com.

ABOUT GLOBALFOUNDRIES

GLOBALFOUNDRIES is the world's first full-service semiconductor foundry with a truly global manufacturing and technology footprint. Launched in March 2009 through a partnership between AMD [NYSE: AMD] and the Advanced Technology Investment Company (ATIC), GLOBALFOUNDRIES provides a unique combination of advanced technology, manufacturing excellence and global operations. With the integration of Chartered in January 2010, GLOBALFOUNDRIES significantly expanded its capacity and ability to provide best-in-class foundry services from mainstream to the leading edge. GLOBALFOUNDRIES is headquartered in Silicon Valley with manufacturing operations in Singapore, Germany, and a new leading-edge fab under construction in Saratoga County, New York. These sites are supported by a global network of R&D, design enablement, and customer support in Singapore, China, Taiwan, Japan, the United States, Germany, and the United Kingdom.

For more information on GLOBALFOUNDRIES, visit <http://www.globalfoundries.com>.

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